REMARKS

The objections to and rejections of the pending claims under 35 USC §112, second paragraph, 35 USC §101, and §102(e) has been obviated by cancelling all of the pending claims 122-145 and replacing them with new claims 146-152. The Examiner should note that the subject matter of the new claims corresponds to the subject matter of the claims as follows:

New Claim:	Previous Claim:
146	123
147	124
	125 cancelled
148	126
149	127
150	128
	129-136 cancelled
151	137
152	138
	139-145 cancelled

1. With regard to Claim Objections

The Examiner objected to the previously pending claims 122-127, 129-138, and 140 on the grounds that had insufficient antecedent basis with regard to the limitation of "the design code", "the design net-list", "the necessary information", "the minimally necessary information", "the back-stage simulation", "the 1st simulation run", "the front-stage simulation", "the design verification method", "the additional code", "the verification run" and "the detection method." Also, the Examiner pointed out that "...includesto..." in Claim 138 should read "...includes to...." In the corresponding new claims 146-149 and 151-152, the word "the" in the pointed-out descriptions is amended to either the word "a" or "an," and the word "...includesto..." is deleted.

2. With Regard to Claim Rejections Based On 35 U.S.C. §112

The Examiner rejected claims 122-124, 126, 129-131, 133-135 under 35 USC §112, second paragraph, because of the inclusion of limitations such as "fast" and "high." In the corresponding new claims 146-149 and 151-152, the words "fast" and high" have been deleted.

3. With Regard to Claim Rejections Based On 35 U.S.C. §101

The Examiner rejected claims 122, 129, 133, 136 on the basis that they were directed to non-statutory subject matter. This rejection has been obviated by effectively cancelling each of these claims, as there is no counterpart between new claims 146-152 and claims 122, 129, 133, 136.

4. With Regard to Claim Rejections Based On 35 U.S.C. §102

The rejection of claims 122-145 as being anticipated by Rajsuman et al. (US Patent No. US 6,678,645 B1) has been obviated in the corresponding new claims be either effectively cancelling the rejected claim, or by re-wording the corresponding new claim to more clearly distinguish the invention from the prior art:

(a) Claim 122

Claim 122 has been effectively cancelled, as there is no counterpart to this claim in new claims 146-152.

(b) Claim 123 (New Claim 146)

New claim 146 corresponds to previously pending claim 123. In new claim 146, some phrases are changed but have same meaning as before (e.g. a number of → one or more, some of → at least one, are decomposed into → consists of, etc.). For your reference, the revised phrase "from a first simulation run when a 1st simulation run is in progress" corresponds to the phrase "during the first simulation run" in claim 123.

In his rejection, the Examiner alleged that the limitation directed to "wherein a necessary information is collected from the 1st simulation run when the 1st simulation run is in progress,..." is disclosed in Col. 7, lines 4-11 of the Rajsuman '645 patent. However, claim 146 also recites

> at least one simulation execution with a test bench consisting of a 1st simulation run as a front-stage simulation and one or more post-1st simulation runs as a back-stage simulation, **wherein a necessary information is collected from the 1st simulation run** when the 1st simulation run is in progress, and **said one or more post-1st simulation runs are executed by using said collected necessary information for obtaining visibility**.

By contrast, in Rajsuman, there is no disclosure or suggestion of any such simulation method. Specifically, in Col. 7, lines 4-11, only discloses that a data file is obtained by executing a logic simulation. It is very much common in the traditional simulation method that a data file such as Verilog/VCD file is obtained for verifying the correctness of design or identifying the design error in logic simulation. Rajsuman does not mention or suggest re-using a data file in other simulation for the specific purpose of visibility.

More generally, the Rajsuman '645 patent concerns an apparatus and verification method to verify the SoC on a divide and conquer basis that utilizes the hierarchical structure of the SoC consisting of IP cores, on-chip buses and glue logic. In Rajsuman, the verification method operates to 1) verify all IP cores individually first, and their on-chip buses and glue logic next, 2) verify core-to-core timing and SoC level timing critical paths, and finally 3) to validate the entire SoC. However, the claimed simulation method does not utilize such a divide and conquer strategy by exploiting the hierarchical structure of the SoC. Both the recited 1st simulation run and the post-1st simulation runs in the claimed simulation method are always carried out with the entire design under verification, i.e. the entire SoC. Hence, the simulation method in the present invention and the simulation method disclosed in Rajsuman are very different in kind from each other. For all of these reasons, new claim 146 is clearly patentable over the Rajsuman '645 patent.

(c) Claim 124 (New Claim 147)

New claim 147 includes the same limitations as previously discussed new claim 146 further recites that "said necessary information consists of the values on all inputs and inout

signals in one or more design objects and the design state of said one or more design objects". This new limitation is expressly supported by the Detailed Description (see in particular lines 21-29 of page 8, and lines 18-28 of page 10 of the PCT publication). Accordingly, all of the arguments submitted on behalf of the patentability of claim 146 apply with even greater force to claim 147.

(d) Claim 125

Claim 125 has been effectively cancelled, as there is no counterpart to this claim in new claims 146-152.

(e) Claim 126 (New Claim 148)

New claim 148 includes all of the same limitations as previously discussed new claim 146 and further recites that "the values on all inputs and inout signals in one or more design objects are saved for the entire simulation time of said 1st simulation run for said necessary information collected from said 1st simulation run." This additional limitation is supported by lines 27-28 of page 8, and lines 22-23 and 33-35 of page 10 of the PCT application. New claim 148 also recites that "one or more design states of said one or more design objects are also saved only at regular intervals in said 1st simulation run for said necessary information collected from said 1st simulation run". This additional limitation is supported by lines 21-25 of page 8, and lines 18-30 of p10 of the PCT application. Finally, the added limitation "said one or more post-1st simulation runs are executed only for the partial simulation time in said entire simulation time of said 1st simulation run" is supported by lines 26-28 of page 10 and lines 24-25 of page 8 of the PCT application. Accordingly, all of the arguments submitted on behalf of the patentability of claim 146 apply with even greater force to claim 148.

(f) Claim 127 (New Claim 149)

New claim 149 corresponds in substance to previously pending claim 127, with only changes of form to render this claim clearer than cancelled claim 127. In the present invention, it is required that the simulation consists of two simulation runs, including simulation runs at a higher level of abstraction and simulation runs at a lower level of

abstraction. Also, in the present invention, it is required that a necessary information is collected when a higher level of simulation run is in progress, and that this necessary information be re-used in the simulation runs at the lower level of abstraction.

In his previous rejection of claim 127, the Examiner asserted that Col. 2, lines 16-22, and FIG. 1 of Rajsuman discloses step-by-step simulation and Col. 2, lines 42-43 discloses that "Development of testbench depends on the function of the core and the target SoC." However, what is actually disclosed in FIG. 1 of Rajsuman is which verification tool is used at a specific kind of abstraction level (i.e. "FIG. 1 illustrates the core design at different levels of abstraction and what type of verification methodology is used today at each level..." Col. 2, lines 16-20.). Rajsuman does not disclose that the simulation result of the higher level of abstraction is re-used in the simulation of the lower level of abstraction. FIG. 1 of Rajsuman neither discloses nor suggests such a simulation method, but simply illustrates the core design at different levels of abstraction and what type of verification methodology is used today at each level. Also, with regard to the statement on Col. 2, lines 42-43 of Rajsuman ("Development of testbench depends on the function of the core and the target SoC.") although SoC consists of a number of cores, it is just a difference of physical size, not a difference of the level of abstraction. For example, the target of verification might be entirely gate-level regardless of whether verifying the core or verifying the SoC. Hence FIG. 1 of Rajsuman does not disclose or suggest the recited back-stage simulation runs using the design at the lower level of abstraction is executed by re-using the necessary information collected from a front-stage simulation run using the design at the higher level of abstraction. For all of these reasons, new claim 149 is clearly patentable over the Rajsuman '645 patent.

(g) Claim 128 (New Claim 150)

New claim 150 is patentable at least by reason of its dependency from new claim 149. Additionally, new claim 150 recites that the simulation results "contain one or more design states of the design at the higher level of abstraction, and said simulation run at the lower level of abstraction is executed in temporally parallel." By contrast, the simulation method in Rajsuman is not performed such a way. In the simulation method of Rajsuman, only the spatially parallel simulation is possible by divide-and-conquer, but the temporally

parallel simulation can**not** be performed. However, with the simulation method in new claim 150, the temporally parallel simulation could be performed.

(h) Claims 129-136

These claims are effectively cancelled, as there are no counterparts to these claims in new claims 146-152.

(i) Claim 137 (New Claim 151)

In his rejection of counterpart claim 137, the Examiner asserted that Col. 2, lines 33-35 and Col.3, lines 18-20 of Rajsuman discloses "the additional code or circuit is instrumented into the design code." However, Col. 2, lines 33-35 of Rajsuman states "(4) Real code testing which is done by running a real application on the design so that any misinterpretation in functionality can be corrected." This implies a simple test after executing the application. Hence Rajsuman discloses only observation or data-obtaining after executing the application, not that an "additional code is instrumented into the design code." Also, Col. 3, lines 18-20 of Rajsuman states that "Static timing analysis is performed on representative netlist of cores that have been emphasized with various technology libraries." This also provides no support for the Examiner's assertion that Rajsuman discloses "the additional code or circuit is instrumented into the design code." In the claimed method, it is always required that the verification method consists of one or more verification runs and the post-debugging simulation, and that the dynamic information is collected when one or more verification runs are in progress and this dynamic information collected in one or more verification runs is re-used in the post-debugging simulation. By contrast, in Rajsuman there is no disclosure of any such simulation method at all, as Rajsuman does not disclose that a data file generated before the design is modified could be re-used in post-debugging simulation for faster post-debugging simulation. For all of these reasons, new claim 151 is clearly patentable over the Rajsuman '645 patent.

(j) Claim 138 (New Claim 152)

New claim 151 includes the limitations of formerly pending claim 138, with the additional limitation "wherein for said collected dynamic information the values on all inputs

and outputs signals in one or more design objects are saved during said one or more verification runs (simulation runs or simulation acceleration runs), and one or more design states of one or more design objects are also saved only at regular intervals during said one or more verification runs (simulation runs or simulation acceleration runs)...." This new limitation is supported by lines 1-6, 12-14 and 22-24 of page 17 of the PCT application. It is also supported by lines 21-29 of page 8, and lines 18-28 of page 10of the PCT publication. The rest of the added phrases are from previously pending 138-143. As new claim 152 depends from new claim 151, all of the arguments submitted on behalf of the patentability of claim 151 apply with even greater force to claim 152.

(k) Claims 139-145

These claims are effectively cancelled, as there are no counterparts to these claims in new claims 146-152.

Now that all of the claims are believed to be allowable, the prompt issuance of a Notice of Allowance and Issue Fee Due is hereby earnestly solicited.

Respectfully submitted,

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